DETAILED ACTION

1. This action is in response to the communication filed on June 18, 2008. Claims 1-31 are pending and have been considered below.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Richard E. Jenkins on August 27, 2008.

The Claims in the application has been amended as follows.

In Claims:

(1) In claim 1, line 27; insert – **bit** – at the beginning of the line before "**stream**".

(2) Replace claim 31 with the following --

31. Method for clock and data recovery of a received serial data bit stream comprising the following steps:

(a) adjusting a sampling time in the center of a unit interval of a received data bit comprising the following substeps:

(a1) generating reference phase signals;

(a2) rotating said reference phase signals in response to a rotation control signal;

(a3) oversampling the received data bit stream with the rotated reference phase signals;

(a4) converting an oversampled data bit stream into a deserialized data stream;

(a5) detecting an average phase difference between the received serial data bit stream and the rotated phase signals by adjusting a phase detector gain depending on a data density of the deserialized data stream to minimize the variation of an average phase detector gain;

(a6) filtering the detected phase difference to generate the rotation control signal;

(b) recovering the received data bit stream comprising the following substeps:

(b1) weighting data samples of the deserialized data stream around the adjusted sampling time;

(b2) summing up the weighted data samples;

(b3) comparing the summed up weighted data samples with a threshold value to detect the logic value of a data bit within the serial data bit stream. --

Allowable Subject Matter

3. Claims 1-31 are allowed.

4. The following is an examiner's statement of reasons for allowance: The present invention is a clock data recovery circuit receiving serial data bit stream and comprising all the below limitations; phase adjustment circuit with, adjustment of a sampling time in the center of a unit interval of the received data bit stream, generating equidistant reference phase signals, a phase interpolation unit, oversampling unit, serial-to-parallel-conversion, binary phase detection unit, a loop filter for filtering the detected average phase difference, data recognition means (DRM-) for recovery of the received data stream which includes a number of parallel data recognition FIR-Filters, weighting unit for weighting data samples of the deserialized data stream, summing unit for summing up the weighted data samples, a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

5. The prior art, Rhee et al. (US 7,197,102) Tuttle et al. (US 6,646,822) and Cranford Jr. et al. (US 7,149,269) discloses a system for clock and data recovery, but fails to disclose that the phase detector comprises means for generating equidistant reference signals over sampling the with rotated interpolated signal and adjusting the gain of the phase detector based on density of deserealized data, and the data recognition comprising a comparator which compares added weighted data samples with a threshold value to detect a logic level of data bit in the received bit stream. It would not been obvious to one of ordinary skill in the art to use the prior art system to make the disclosed system in the present invention. The distinct features have been added to the independent claims 1, and 31. Therefore, rendering them allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Terminal Disclaimer

6. The terminal disclaimer filed on June 18, 2008 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent # 7,292,662 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Cranford Jr. et al. (US 7,149,269) discloses a system and method for clock and data recovery with calibrated sampling with adjustable signal.

b. Sugawara et al. (US 2006/0181797) discloses system and method for timing recovery in communication systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HIRDEPAL SINGH whose telephone number is (571)

270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off) 8:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. S./
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611